ANALYSIS AND DESIGN OF PARTIAL POSITIVE FEEDBACK CHARGE-PUMP CIRCUITS FOR PLL APPLICATIONS

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ABSTRACT

The analysis and design of two novel CMOS charge-pump circuits for PLL applications is presented. Based in partial positive feedback and current reuse, the switching speed is increased and the total power consumption is reduced. The proposed circuits are capable to operate at 2V for a frequency of 100 MHz. Simulation results for a 0.35 µm AMS technology with BSIM3V3 LEVEL=49 model parameters, show the feasibility of both structures for low voltage and high frequency applications.

1. INTRODUCTION

In recent years, the fast growth of the cellular communication systems, has motivated an increasing demand of high-performance RF integrated circuits [1]. One of the most important blocks of those systems is the local oscillator (LO). The need of a well defined and highly stable signal for the local oscillator, makes necessary the use of phase locked loop techniques in order to satisfy the stringent requirements of standards like GSM [2]. Among different PLL topologies, the charge-pump PLL is mainly utilized because the advantages offered versus traditional realizations [3]. Phase noise is the most critical parameter that an integrated LO must satisfy. If a PLL is used, increasing the loop bandwidth helps to reduce it. However, this last requires a high frequency charge pump.

2. TRADITIONAL CURRENT STEERING CHARGE-PUMP CIRCUITS

Figure 1 shows the concept of a charge-pump circuit. It consists of two switched current sources driving a capacitor. The switching is realized by means of a three-state phase-frequency detector (PFD). When the UP signal is high and DWN is low (first state), current source I1 is steered trough CL, increasing Vo.

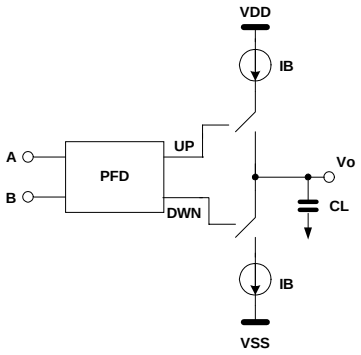

Figure 1. The PFD and charge-pump combination.

On the other hand, when UP is low and DWN is high (second state), I2 sinks current and the output voltage is decreased. Finally, when both UP and DWN are low (third state), the net current is zero and Vo remains constant. When MOS transistors are employed to replace the ideal switches, a voltage error component is generated due to the non-ideal behavior of MOS switches (fig. 2). These errors, called charge injection and clock-feedthrough, cause a jump in the stored voltage on CL, which is transformed in phase noise and spurious tones in the VCO output [4].

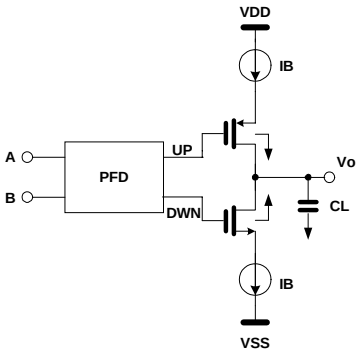

Figure 2. Charge injection and clock-feedthrough errors produced by MOS switches.

Recently, some topologies have been proposed in order to improve the discussed problems. Current steering techniques have been utilized because they allow achieve both fast switching speed and low charge injection errors. Figure 3 shows the basic circuit proposed in [5,6,7]. It consists in a current switch (M1-M2), with a current mirror as load (M3-M4) and a pull-up current mirror (M5-M6). The current switch is driven by the differential signal provided by the PFD. Thus, when the signal in UP+ is greater than UP-, the current source IB is steered on M2. The difference between this current and Is is mirrored by M3 and M4, producing the charge/discharge current. On the other hand, when Up+ is lower than UP-, the current is deviated on M1. The pull-up circuit is used to increase the charge speed of node A. If this circuit is not used, when the current of the input pair is steered though M1, M3 produces a temporal current, which modulates the VCO, generating spurious tones. Since the associated time constant for this process depends of the parasitic capacitance and resistance seen by the node A, this is called a slow path. Although the improved performance over the basic cell, the previous circuit presents several drawbacks. First, when the current source IB is steered through M1, this current is wasted since it is not any more utilized. Furthermore, the current source Is reduces the total output current and must be enough small in order to not increase the power consumption. Finally, since this current is only used for a specific time, an unavoidable static power consumption is produced.

In this paper, design techniques for current steering charge-pump circuits intended for low-voltage and high frequency applications are proposed. These techniques allow obtain a faster switching speed and lower power consumption compared with similar previously reported structures.

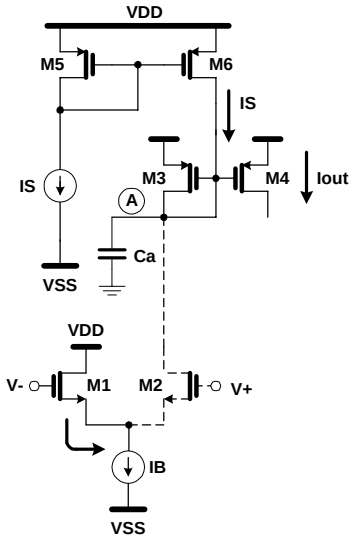

Figure 3. Basic circuit proposed by Chang et al.

3. THE POSITIVE FEEDBACK AND CURRENT REUSE CHARGE-PUMP

The proposed topology is shown in figure 4. It makes use of the current source IB when it is steered to M1, avoiding the need of Is and thus saving power. Furthermore, since the current injection is greater than the previous structure, M4 is turned off faster. However, the problem of the slow path still continues, now at node B. To overcome this, a pull-up transistor (M7) is added. The final configuration is a simple partial positive feedback amplifier with gain enhancement [8], where the switching speed is increased. Figures 3 to 5 show the evolution of the proposed topology. The amount of positive feedback is given by:

$$\alpha = (W/L)_5 / (W/L)_6 \quad (1)$$

The switching speed of the circuit depends of the parasitic capacitance associated to node A and the current source IB. The capacitance on node A is given by:

$$C_A \approx Cgs_3 + Cgs_4 + Cgs_7 + Cdb_2 + Cdb_5 + Cdb_7 \quad (2)$$

From equation (1), it can be deducted that a maximum value for α must be 1, or the circuit becomes a latch. A practical value for this parameter is 0.75 [9]. The switching point of the input differential pair is given by:

$$V_{SW} = \sqrt{2}(V_{GS1} - V_{T1}) = \sqrt{2}V_{DSAT1} = \sqrt{\frac{4IB}{Kn(W/L)_1}} \quad (3)$$

In this way, a trade-off between switching point and capacitance must be realized. Furthermore, for low-voltage operation, VDD must be satisfy:

$$V_{DD} \geq V_{GS3} + V_{DSAT2} + V_{DSATIB} \quad (4)$$

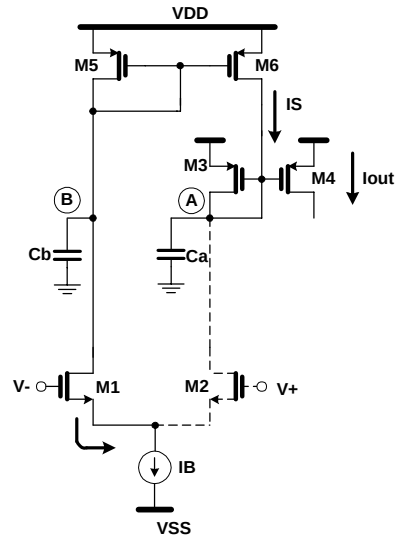

Figure 4. Modification for current reuse.

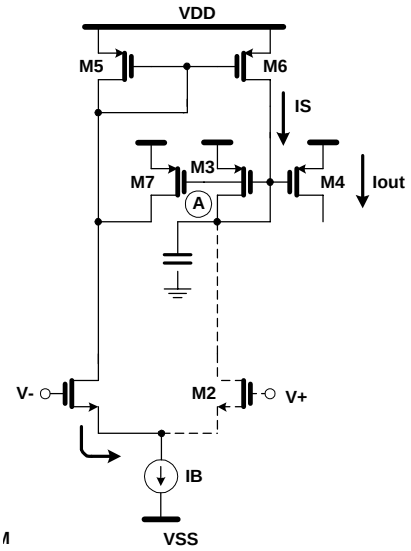

Figure 5. Final basic topology with partial positive feedback and current reuse.

Interestingly, the total area for the basic cell remains almost the same, because topologically, the transistor implementing the current source Is has only been transformed into the M7 transistor, with the advantage of a more symmetrical layout, as shown in figure 6.

4. SIMULATION RESULTS

In order to show the capabilities of the proposed technique, the design of two charge-pumps is presented. Both designs are compared versus similar current steering structures [5,6,7]. The generation of differential signals for the PFD is achieved by using a Shoji´s delay balanced chain [10].

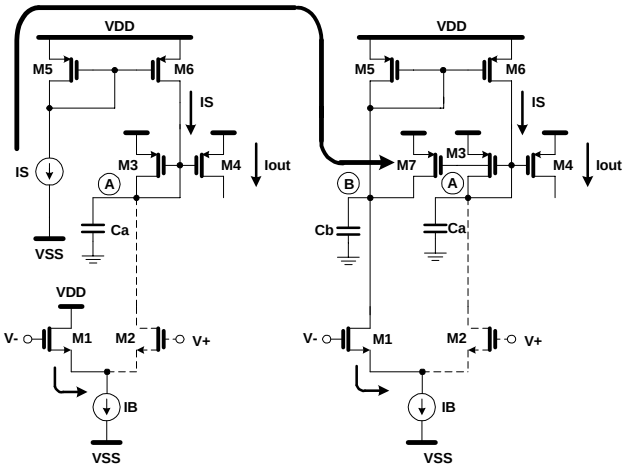

Figure 6. A Topological description of the proposed technique.

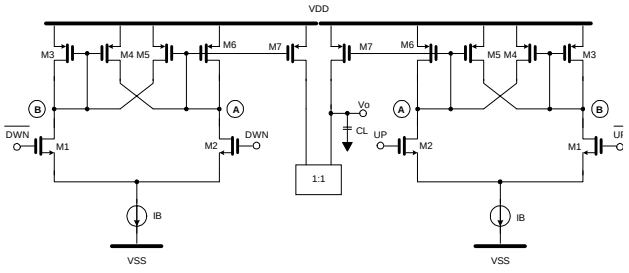

Figure 7. NMOS charge-pump circuit.

The first charge-pump is composed of two basic cells with a 1:1 current converter (fig.7). In the present work, a simple current mirror was used to implement the 1:1 converter, but other current mirror topologies can also be used. Figure 8 shows the output current on CL during the pumping-down phase, while figures 9 and 10, the pumping-up and pumping-down waveforms respectively. Despite a new slow path is introduced by the inclusion of the current mirror, this problem can easily be solved with a small discharge transistor [11]. Finally, a temperature analysis from 10° to 60° Celsius degrees was performed, showing a maximum deviation of only 10 mV over the nominal point. These results are shown in figure 10.

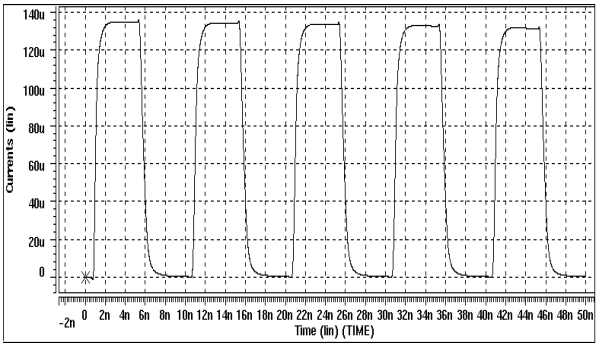

Figure 8. Output current in the pumping-down phase (f=100 MHz, VDD=2V).

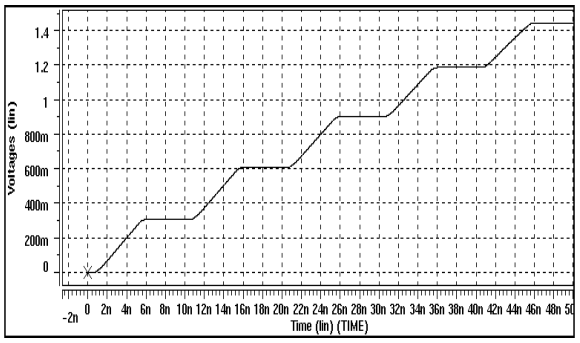

Figure 9. Pumping-up (f=100 MHz, VDD=2V).

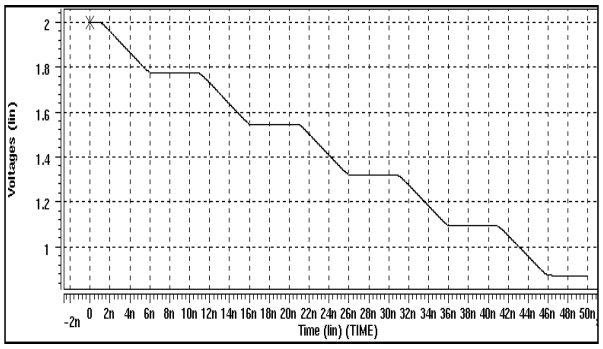

Figure 10. Pumping - down of the first proposed charge-pump.

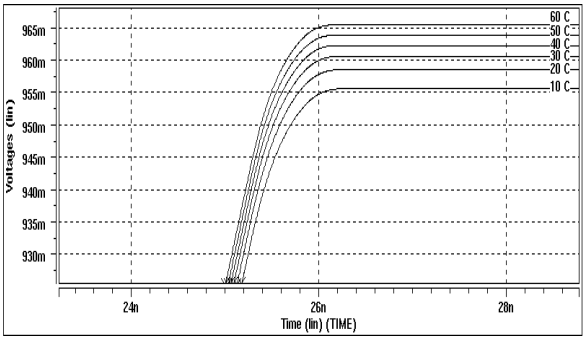

Figure 11. Variation on Vo for temperature changes (T=10°C to 60°C).

Figure 12 shows the second charge pump topology. This circuit avoids the need of a 1:1 converter, by using complementary cells. In the same way that [6], this configuration is capable to generate well-controlled short current pulses. To realize this, the delays in N and P paths must be equalized, thus mandating a careful design. As a final note, this circuit introduces low switching noise, thus been desirable for low noise applications. All the simulations were realized for a 0.35 μm CMOS technology with BSIM3V3 Level=49 model parameters, for a frequency of 100 MHz and VDD=2V.

5. CONCLUSIONS

The analysis and simulation of two novels CMOS charge pump circuits has been presented. Positive feedback and current reuse are used to obtain fast switching speed and low power consumption simultaneously, outperforming previously reported structures. Simulation results show that the proposed circuits are capable of operate at low voltage and high frequency without significant degradation. Furthermore, a maximum error of 10 mV for a 10° to 60° C temperature range makes the circuit only slightly dependent on temperature variations. Those features make the presented structures well suitable for wide-band & low-voltage RF PLL applications.

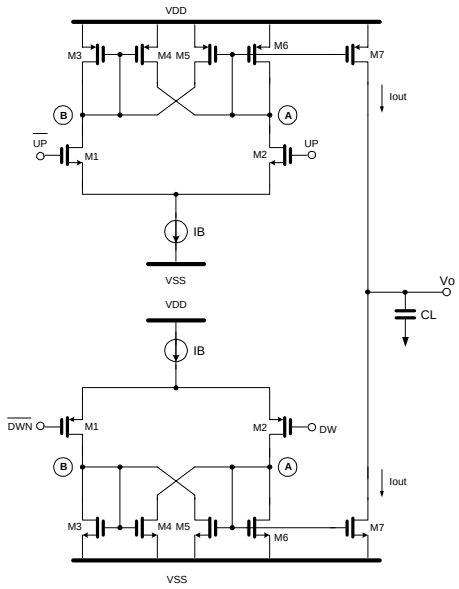

Figure 12. Complementary charge-pump circuit.

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