Switched Op-Amp ΔΣ Modulator with 74-dB Dynamic Range Based on Folded Cascoded Switched OTA

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ABSTRACT

The design of a second-order switched-opamp ΔΣ modulator, with an analog half-delay block in the forward path is presented. The main objetive of this paper is oriented to demonstrate the feasibility of building a ΔΣ modulator based on a fully differential folded-cascode OTA, switched at 16MHz with a single 3.3 V power supply. The switching process is performed by current deviation at the OTA output stage, instead of turning off its bias current or to interrupt the current path from the power supplies. Simulated results for the ΔΣ modulator using HSPICE, show a 74-dB dynamic range in a 125-kHz bandwidth and a 67-dB peak signal-to-noise ratio for a 2.8-mW power consumption.

Keywords: *data converters, switched capacitor circuits, switched op-amp technique*

1. Introduction

In switched capacitor (SC) circuits, the OTA which is configured as an integrator is the principal building block for SC filters and SC ΔΣ modulators. The fully differential folded-cascode OTA satisfies the gain and speed requirements for SC circuits applications [1]. For SC circuits at low voltage, the switched op-amp (SO) technique is a good alternative, without the use of neither voltage multipliers nor low V_T devices to drive the switches.

In a SC integrator, the switches are classified as: switches that have one terminal tied to a reference level and switches that pass the entire signal range, which are typically found at the output of the amplifier. The former can always be turned on, but the latter are identified as problematic switches [2, 3, 4]. Therefore, the basic idea of the SO technique is to eliminate the switches connected to the output of an OTA in a SC integrator, by connecting the sampling capacitor directly to the OTA output as shown in Fig. 1.

When the OTA is not integrating, its output is shorted to the analog ground. This fact requires that the OTA, or at least its output stage, to be inactive during the phase in which it is not integrating.

Some designs related to SO are summarized in the following:

In [2] a Miller op-amp was used as SO, and could be switched at 115 kHz with a 1.5 V power supply by turning off its bias currents. However, this technique limits the sampling frequency, because the diode connected side of the bias current mirror must be charged up with a constant current, and consequently the maximal switching speed would then be reduced.

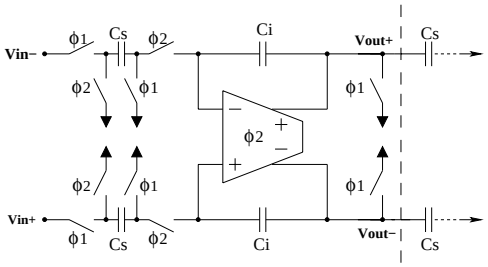

Fig. 1. A switched opamp integrator.

The technique proposed in [3], consist of switching a class AB OTA by interrupting completely the current path from the power supplies V_{DD} and V_{SS} to the circuit, with switches from the external node to an internal supply nodes. In this case the sampling frequency was of 1.538 MHz for a 0.9 V supply voltage.

In [4], the op-amp uses a two-stage topology where only the output stage is turned on and off, by interrupting the current path from the power supplies. This allows the use of a higher sampling frequency. The op-amp could be switched at 1.8 MHz with a single 1 V supply voltage, and with 1.2 V supply voltage a maximum sampling frequency of 9 MHz was reached.

In [5] the output stage of an op-amp, could be switched to the high impedance state by opening the switches between the current sources and ground. The transient simulation presented is for 1 V supply voltage, and a sampling frequency of 1 MHz.

In [6], a single ended folded cascode OTA is switched at 10 kHz from a single 5 V supply voltage, and it is used in a sample-and-hold circuit.

With the switching technique reported at [9] and described here, the fully differential folded-cascode OTA can be switched up to 16 MHz with a single 3.3 V supply voltage.

2. Fully differential folded-cascode switched OTA.

The proposed switching technique for the fully differential folded-cascode OTA symmetrically compensated [8], is based on the output stage current deviation [9] instead of turning off the bias current, or to interrupt the current path from the power supplies, as is the case for the SO previously cited [2, 3, 4, 5, 6]. The Fig. 2, shown the fully differential folded-cascode switched OTA reported at [9].

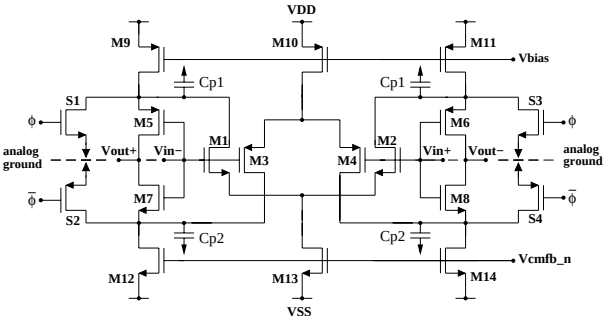

Fig. 2. Fully differential folded-cascode switched OTA.

The transistors S_1-S_4 used as switches, perform the current deviation in order to turn off the OTA output stage only. The drain of the NMOS switches S_1 and S_3, are connected to the source of the PMOS transistors M_5 and M_6, while the drain of the PMOS switches S_2 and S_4, are connected to the source of NMOS transistors M_7 and M_8. The source of the transistors S_1-S_4 are connected to analog ground. The OTA output stage is turned off when the transistors S_1-S_4 are turned on. At this moment, the source of the M_5-M_8 are pulled to the analog ground and V_{GS5}-V_{GS8} are small compared with its V_T, making the conductivity of M_5-M_8 very small, and the current is deviated to the transistors S_1-S_4.

On the other hand the drain voltages of transistors M_1-M_4 are pulled to the analog ground, so that $V_{DS1} \approx V_{GS1}$, $V_{DS2} \approx V_{GS2}$, $V_{DS3} \approx V_{GS3}$ and $V_{DS4} \approx V_{GS4}$. Therefore the transistors M_1-M_4 are in the saturation region.

With this switching technique, the sampling frequency depends on the time constant given by [9]

$$\tau_1 = \frac{C_{p1}}{g_1} \tag{1}$$

and

$$\tau_2 = \frac{C_{p2}}{g_2} \tag{2}$$

with

$$g_1 \approx g_{s1} + g_{ds5} + g_{ds9} \tag{3}$$

and

$$g_2 \approx g_{s2} + g_{ds7} + g_{ds12} \tag{4}$$

Where g_{s1} (g_{s3}), g_{s2} (g_{s4}), g_{ds5} (g_{ds6}), g_{ds7} (g_{ds8}), g_{ds9} (g_{ds11}) and g_{ds12} (g_{ds14}) are the output conductances of S_1 (S_3), S_2 (S_4), M_5 (M_6), M_7 (M_8), M_9 (M_{11}) and M_{12} (M_{14}), respectively.

C_{p1} and C_{p2} are the parasitic capacitors associated to the source of M_5 (M_6) and M_7 (M_8), respectively.

If $C_{p1} \approx C_{p2}$ and $g_1 \approx g_2$ then $\tau_1 \approx \tau_2$, thus the sampling frequency for the switched OTA is given by:

$$f_S = \frac{g_1}{2\pi C_{p1}} \tag{5}$$

A Common Mode Feedback (CMFB) scheme, especially designed for the SO technique reported at [3] and used here, is shown in Fig. 3.

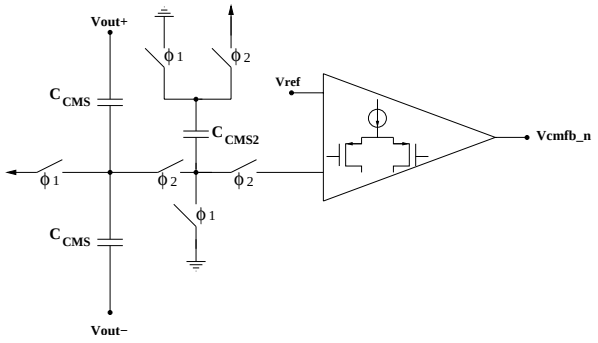

Fig. 3. Common mode feedback.

It consists of an error-amplifier-based CMFB without divider. The capacitors C_{CMS} sample the

common mode, while C_{CMS2} gives a DC offset to level shift the CM sample. The error amplifier shown on the right consists basically of a differential pair.

Fig. 4 shows the magnitude and phase responses for the switched OTA during the on-phase [9], for a simulation with HSPICE.

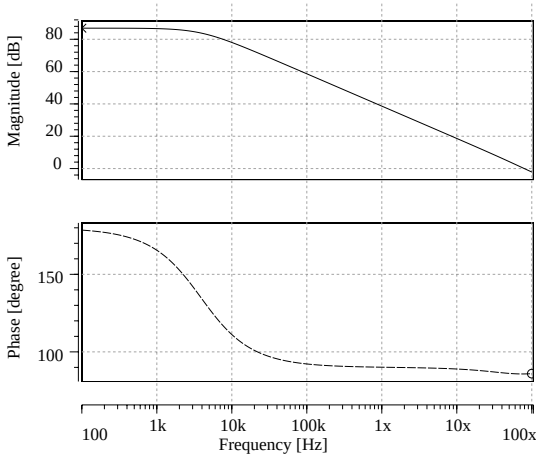

Fig. 4. Frequency response for the folded-cascode switched OTA.

All the simulated results for the switched OTA [9], are shown in Table 1.

Table 1. Simulated Performance Characteristics.

Parameter	Value	Units
DC Gain	87	dB
GBW	79	MHz
Phase margin (1.2pF)	85	°
Settling time (0.1% and 1.2pF)	25	ns
Slew rate	36	V/μs
Supply voltage	3.3	V
Power consumption	405	μW

In Fig. 5, the drain currents of the transistors M_5 (M_6) and M_7 (M_8) are presented [9]. The currents for transistors M_5 and M_7 are switching at 16 MHz from 0 μA to -46 μA and +46 μA, respectively. From transient simulation shown in Fig. 5 the drain currents of M_5 and M_7 are settled properly, maintaining an adequate operation in on-phase.

Fig. 6 shown a transient simulation of the integrator of the Fig. 1, where the integrator action for a constant input can be seen in the graph, which shown the differential output voltage.

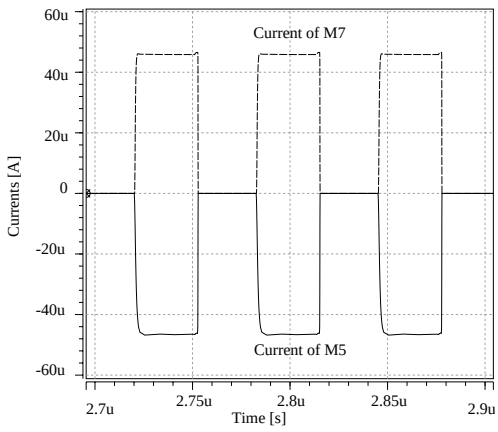

Fig. 5. Drain currents of transistors M_5 and M_7.

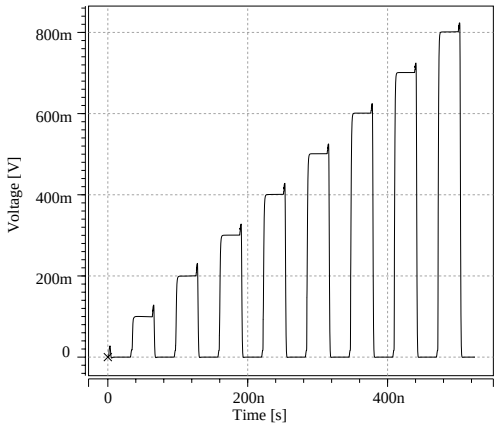

Fig. 6. Integrator output voltage.

3. SO $\Delta\Sigma$ Modulator Design.

The block diagram of the second order $\Delta\Sigma$ modulator is shown in Fig. 7. The $\Delta\Sigma$ modulator makes use of full-delay integrators, and the transfer function is

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{6}$$

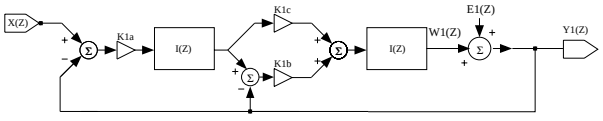

Fig. 7. Second order $\Delta\Sigma$ modulator topology.

The basic SO integrator cell presents only a half-delay to the signal. The transfer function is

$$H(z) = \frac{z^{-1/2}}{1 - z^{-1}} \tag{7}$$

If a full-delay integrator is required, the integrator can be preceded by an analog half-delay block [2]. This can be implemented by a switched-capacitor amplifier with a unity gain. Since the purpose of this design is to demonstrate the feasibility of building a SO $\Delta\Sigma$ modulator based on a fully differential folded-cascode switched OTA, we chose the SC fully differential topology shown in Fig. 8, which is based on an analog half-delay block in the forward path. The fully differential configuration is adopted in order to ensure high power supply rejection ratio, reduce the offset voltage from clock feedthrough, improve linearity and increase dynamic range.

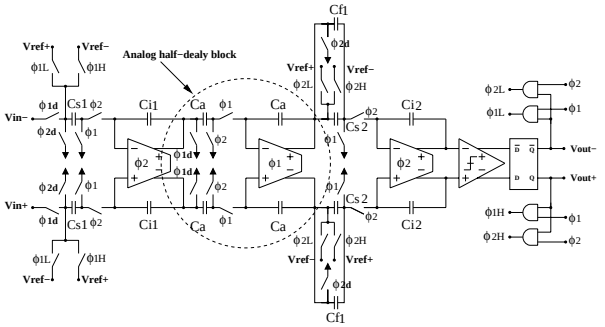

Fig. 8. Second order SO $\Delta\Sigma$ modulator.

The SO $\Delta\Sigma$ modulator consists of three OTAs. The first and third OTAs implement the half-delay integrator, and the second OTA performs the function of the half-delay element.

There are two nonoverlapped clock phases, in normal and delayed versions, in order to reduce signal-dependent charge injection. ϕ_1 and ϕ_2 are non overlapping clock phases and are used for the switches at the opamp input. The clock phases ϕ_{1d} and ϕ_{2d} are used to switch the capacitors to the input signals of the integrator, and they are turned off slightly before ϕ_1 and ϕ_2 respectively to reduce the signal dependent clock feedthrough.

For the first half-delay integrator, C_{S1} is used to sample both the input signal and the reference signal [7]. In this way we can save chip area and increase the speed since the feedback factor is larger and the total load is smaller.

The integrator gains are chosen to give signal swings at the OTA outputs that are equal to or slightly less than the swing of the feedback signals of the DAC. Suitable values for capacitors are summarized in Table 2

The LAYOUT of the SO $\Delta\Sigma$ modulator is shown in Fig. 9

Table 2. Capacitor Values for SO $\Delta\Sigma$ Modulator.

Capacitor	Value (pF)
C_{s1}	1.00
C_{i1}	2.00
C_{s2}	0.25
C_{i2}	1.00
C_{f1}	0.25
C_a	0.25

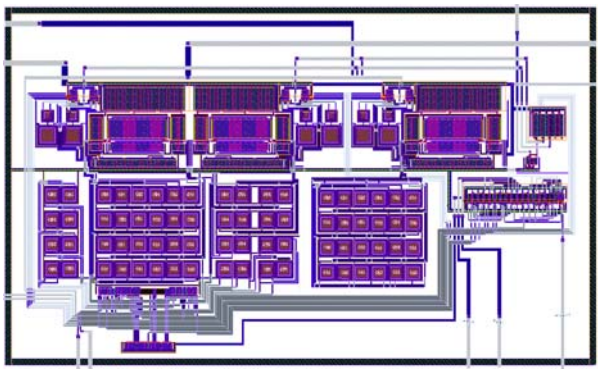

Fig. 9. LAYOUT of second order SO $\Delta\Sigma$ modulator.

4. Simulated Results.

The SO $\Delta\Sigma$ modulator in Fig. 8, was designed using a 0.6μm CMOS technology and was simulated with HSPICE. The SO $\Delta\Sigma$ modulator was modeled and simulated using MATLAB. The reference levels V_{ref+} and V_{ref-} of the DAC are +1 and -1, respectively. A sinusoidal input signal with amplitude of 0.65 full-scale (FS) and a frequency of 125 kHz is used. The modulator-sampling rate was 16 MHz.

The power spectral density of the output signal for 32k-point is shown in Fig. 10, and the Fig. 11 shows the simulated SNR and the SNDR from HSPICE. Table 3 summarizes the performance characteristics for SO $\Delta\Sigma$ modulator designed.

5. Conclusion.

A second-order SO $\Delta\Sigma$ modulator with an analog half-delay block in the forward path, which is based on a fully differential folded-cascode OTA switched at 16MHz has been presented. The main contribution of this work was to demonstrate the feasibility of building a $\Delta\Sigma$ modulator based on a fully differential folded-cascode switched OTA. The modulator achieves a 12-b dynamic range and a signal bandwidth of 125 kHz in a 0.6-μm CMOS technology.

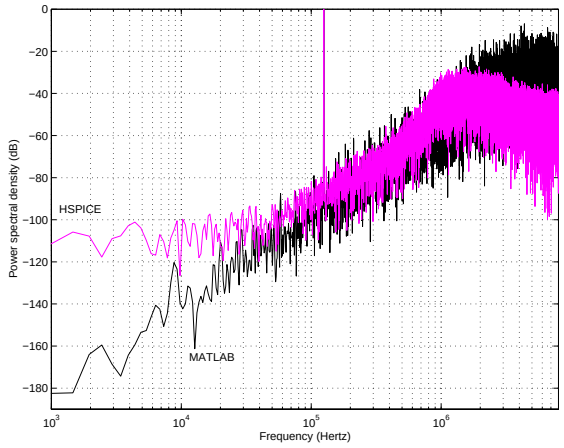

Fig. 10. Power spectral density of SO ΔΣ Modulator.

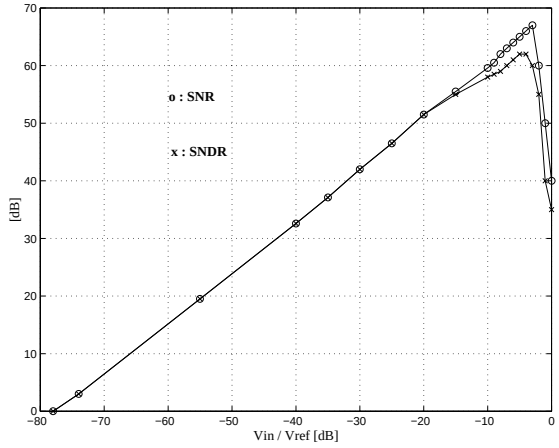

Fig. 11. SNR and SNDR of SO ΔΣ Modulator.

Table 3. Performance Characteristics.

Parameter	Value	Units
DR	74	dB
peak SNR	67	dB
peak SNDR	63	dB
Samplig Frequency	16	MHz
Signal Bandwidth	125	kHz
DAC V_{ref}	± 1.0	V
Signal Amplitude	0.65 FS	V
Supply Voltage	3.3	V
Power Consumption	2.8	mW

References

[1] Tat C. Choi, Ronald T. Kaneshiro, Robert W. Brodersen, Paul R. Gray, William B. Jett, and Milton Wilcox, *"High-frequency CMOS switched-capacitors filters for communications application"*, IEEE J. Solid-State Circuits, Vol. SC-18, No. 6, pp. 652-664, December 1983.

[2] J. Crols, and M. Steyaert, *"Switched-opamp: An approach to realize full CMOS switched-capacitors circuits at very low power supply voltages"*, IEEE J. Solid-State Circuits, Vol. 29, No. 8, pp. 936-942, August 1994.

[3] V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, *"900 mV differential class AB OTA for switched opamp applications"*, Electronic Letters, Vol. 33, No. 17, pp. 1455-1456, August 1997.

[4] A. Baschirotto, and R. Castello, *"A 1V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing"*, IEEE J. Solid-State Circuits, Vol. 32, No. 12, pp. 1979-1986, December 1997.

[5] M. Waltari, and K. Halonen, *"Fully differential switched opamp with enhanced common mode feedback"*, Electronic Letters, Vol. 34, No. 23, pp. 2181-2182, November 1998.

[6] Liang
Dai, and Ramesh Harjani , *"CMOS switched-op-amp-based sample-and-hold circuit"*, IEEE J. Solid-State Circuits, Vol. 35, No. 1, pp. 109-113, January 2000.

[7] S.R.Norsworthy, R.Schreier, and G.C.Temes, *"Delta-Sigma Data Converters: Theory, Design and Simulation"*, IEEE Press, 1997.

[8] G. Espinosa-Flores-Verdad, and R. Salinas-Cruz, *"Symmetrically compensated fully differential folded-cascode OTA"*, Electronic Letters, Vol. 35, No. 19, pp. 1603-1604, September 1999.

[9] R. Salinas-Cruz, and G. Espinosa-Flores-Verdad, *"A Folded-Cascode Switched OTA Based on Current Deviation"*, Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 17-19, 2002.